

FORM PT01449  
(REV. 8-83)

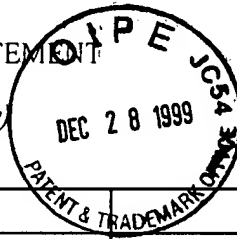
U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.  
HARI.006USF

SERIAL NO.  
08/789,421

INFORMATION DISCLOSURE STATEMENT

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APPLICANT  
ELIYAHOU HARARI et al.

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
<i>W</i>	B25	wo 8 5/ 0 3 5 8 3	8/15/85	PCT			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>W</i>	C28	Qualogy, Inc. "QPC-5213, QPC-5212, QPC-5211 Solid-State Disk Emulator", Configuration Manual, 1987.
<i>W</i>	C29	"SCSI/MEM NOVRAN and EPROM disk drive on SCSI", 1 page, date unknown.
<i>W</i>	C30	"Introduction from the Third European Solid-State Circuits Conference Organizing Committee", IEEE Journal of Solid-State Circuits, Vol. SC-13, No. 3, pg. 282, June 1978.
<i>W</i>	C31	Aubusson et al., "Wafer-Scale Integration-A Fault-Tolerant Procedure", IEEE Journal of Solid-State Circuits, Vol. SC-13, No. 3, pg. 339-344, June 1978.
<i>W</i>	C32	Oka et al., "Hitachi SV501C Series Semiconductor Storage Devices", Hitachi Review, Vol. 39, No. 5, pg. 267-272, October 1990.
<i>W</i>	C33	Hsia, Yukun, "Memory Applications of the MNOS", 1972 WESCON Technical Papers, Vol. 16, pg. 1-5, September 19-22, 1972.
<i>W</i>	C34	Hsia et al., "A Reconfigurable Interconnect for In-Silicon Electronic Assembly", 32nd Electronic Components Conference, San Diego, California, pg. 7-16, May 10-12, 1982.
<i>W</i>	C35	"6M20 Disk Emulator Manual", Mesa Electronics, Version 1.1, 1987.
<i>W</i>	C36	"8M20 Disk Emulator Manual", Version 1.2, Mesa Electronics, 1989.
<i>W</i>	C37	"6M20 RAMdisk Driver - Hard disk Replacement", Mesa Electronics, Revision History, 1987-1989.
<i>W</i>	C38	"6M20 Block I/O Functions", Mesa Electronics, Revision History, 1987-1989.
<i>W</i>	C39	"Solid State Crash Survivable Flight Data Recorders for Mishap Investigation", pg. 34-63, publication date and source unknown.
<i>W</i>	C40	"Electrically Erasable PROM", Xicor Data Book, pg. 3-177 thru 3-179, May 1987.

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8/6/80

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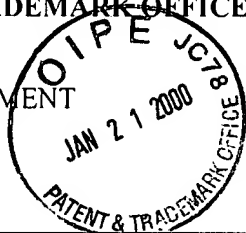
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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER								DATE	NAME	CLASS	SUB CLASS	FILING DATE
LC	AE6	4	1	1	5	9	1	4		9/26/78	Harari			
LC	AE7	4	4	8	9	3	5	1		12/18/84	d'Alayer de Costemore d'Arc			
LC	AE8	4	7	4	2	2	1	5		5/3/88	Daughters et al.			
LC	AE9	4	7	6	8	1	9	3		8/30/88	Takemac			
LC	AF1	4	8	6	2	2	0	0		8/29/89	Hicks			
LC	AF2	5	0	9	3	7	3	1		3/3/92	Watanabe et al.			
LC	AF3	5	1	0	1	2	4	9		3/31/92	Hijiya et al.			
LC	AF4	5	2	2	2	0	4	6		6/22/93	Kreifels et al.			

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		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
LC	B26	wo	8	8	0	9	0	1	9	2/17/88	PCT			

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LC	C41	Geideman, et al., "Silicon Machine - A Reconfigurable On-The-Wafer Interconnect Architecture for VLSI Systems", Naval Air Development Center, Warminster, PA, pg. 235-237.												
LC	C42	Hsia, et al., "Highly-Reliable Semiconductor Mass Memory", 1979 IEEE, pg. 881-887.												
LC	C43	Hsia, et al., "Reconfigurable Interconnect for In-Silicon Electronic Assembly", Naval Air Development Center, Warminster, PA, 1982, pg. 7-16.												
LC	C44	Hsia, Yukun, "Wafer Scale Integration", University of Santa Clara, Santa Clara, California, June 7, 1984.												
LC	C45	Hsia, Yukun, "Nonvolatile Semiconductor Memories", University of Santa Clara, Santa Clara, California, May 11, 1984.												

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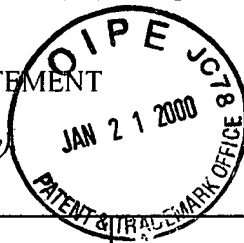
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SERIAL NO. 88/789,421

## INFORMATION DISCLOSURE STATEMENT

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ELIYAHOU HARARI, et al.FILED  
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2785

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>WCH</i>	C46	Gosney, W. Milton, "DIFMOS-A Floating-Gate Electrically erasable Nonvolatile Semiconductor Memory Technology", IEEE Transactions on electron Devices, Vol. ED-24, No. 5, May 1977, pg. 594-599.
<i>WCH</i>	C47	Guterman, et al., "An Electrically Alterable nonvolatile Memory Cell Using a Floating-Gate Structure, IEEE Journal of Solid State Circuits, Vol. SC-14, No. 2, pp. 498-508, April 1979.
<i>WCH</i>	C48	Cacharelis, et al., "A Single Transistor Electrically Alterable Cell", IEEE Electron Device Letters, Vol. EDL-6, No. 10, October 1985, pg. 519-521.
<i>WCH</i>	C49	"Non-Volatile High-Speed Electronic Storage for the IBM Personal Computer", IBM Technical Disclosure Bulletin, Vol. 28, No. 8, January 1986, pg. 3395-3396.

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	<b>APPLICANT</b> ELIYAHOU HARARI et al.	
	<b>FILED</b> January 29, 1997	<b>GROUP</b> 2785

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*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>LYH</i>	AF5	4 0 0 7 4 5 2	2/8/77	Hoff, Jr.			
<i>LYH</i>	AF6	3 8 1 0 1 2 7	5/7/74	Hoff, Jr.			
<i>LYH</i>	AF7	3 8 2 1 7 1 5	6/28/74	Hoff, Jr. et al.			
<i>LYH</i>	AF8	3 5 9 3 0 3 7	7/13/71	Hoff, Jr.			
<i>LYH</i>	AF9	5 1 7 2 3 3 8	12/15/92	Mehrotra et al.			
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

### OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

<i>LYH</i>	C50	Declaration of Yukun Hsia, Ph.D. with Exhibits A-H, dated February 11, 2000.
<i>LYH</i>	C51	Declaration of W. Milton Gosney, Jr., with Exhibits 2-8, dated February 11, 2000.
<i>LYH</i>	C52	Deposition of Yukun Hsia, Ph.D., January 27, 2000, page 1-171.
<i>LYH</i>	C53	Hsia et al., "Impact of MNOS/AWSI Technology on Reprogrammable Arrays", McDonnell Douglas Corporation, May 26-27, 1981, pg. 1-16.
<i>LYH</i>	C54	Zales, Saul, "Flash Memories Change System Design Fundamentals", Wescon/88 Electronic Show and Convention, November 15-17, 1988, Anaheim, California, pg. 1-6.
<i>LYH</i>	C55	Norris, Rich, "Flash Technology: Bridging the Gap Between EPROMS and EEPROMS", Wescon/88 Electronic Show and Convention, November 15-17, 1988, Anaheim, California, pg. 1-4.
<i>LYH</i>	C56	Mehrotra et al, "Serial 9MB Flash EEPROM for Solid State Disk Applications", IEEE Symposium on VLSI Circuits Digest of Technical Papers, Feb. 1992, pp. 24-25.
<i>LYH</i>	C57	Lee et al., "An 18MB Serial Flash EEPROM for Solid-State Disk Applications", IEEE Symposium on VLSI Circuits Digest of Technical Papers, April 1994, pp.59-60.
<i>LYH</i>	C58	"Memory Components Handbook", 1990

<b>EXAMINER</b>  <b>LY V. HUA</b> <b>PRIMARY EXAMINER</b>	<b>DATE CONSIDERED</b> 8/6/00
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		<b>FILED</b> January 29, 1997	<b>GROUP</b> 2785

**U. S. PATENT DOCUMENTS**

*EXAMINER INITIAL	AG1	4	1	9	3	1	2	8	DATE	NAME	CLASS	SUB CLASS	FILING DATE
BW	AG1	4	1	9	3	1	2	8	3/11/80	Brewer			
BW	AG2	4	0	9	9	0	6	9	7/4/78	Cricchi et al.			
		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUB CLASS	TRANS? (YES/NO)

**OTHER DOCUMENTS** *(Including Author, Title, Date, Pertinent pages, Etc.)*

BW	C59	Hsia et al., "Adaptive Integrated Technology Development: Vol. 3: Mass Memory System Description", Part 1, 23 May 1979.
BW	C60	Iwata et al., "A High-Density NAND EEPROM with Block-Page Programming for Microcomputer Applications", IEEE Journal of Solid-State Circuits, vol. 25, No. 2, April 1990, pg. 417-418.
BW	C61	"Wafers to Challenge disks, bubbles ?", Electronics, August 16, 1979.
BW	C62	Momodomi et al, "New Device Technologies for 5V-ONLY 4mb EEPROM with Nand Structure Cell", ULSI Research Ctr, Toshiba Corp, Japan, IEDM, pp. 412-415.
BW	C63	"Advanced Memory (BORAM) Application Using MNOS Technology", Litton Systems, Inc., March 1972.
BW	C64	"Project 779: Design Review", 19-20 January 1982.
BW	C65	Hsia et al., "MDAC Solid-State Memory Development", McDonnell Douglass Astronautics Company, 19 May, 1980.
BW	C66	Brewer et al., "New Storage Medium Saves \$22 Million: Smaller, Lighter, More Reliable", Reprint from U.S. Army ManTech Journal, vol. 4, No. 4, pg. 1-14.
BW	C67	Brewer, J.E., "Test Report: Initial BORAM 6008 Samples: Contract N00421-77-R-0198: BORAM 8K Memory Chip", Naval Air Test Center, Patuxent River, Maryland, 6 March, 1978.

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